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INFORMATION DISCLOSURE STATEMENT BY APPLICANT

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Sheet 1 of 1

Complete If Known	
Application Number	
Filing Date	07/14/2003
First Named Inventor	Keith E. Kunz, et al.
Group Art Unit	
Examiner Name	
Attorney Docket No.	TI-33676.1

U.S. PATENT DOCUMENTS

Exam. Initials*	Cite No.[1]	U.S. Patent Document Number	U.S. Patent Document Kind Code[2] (if known)	Name of Patentee or Applicant of Cited Doc.	Date of Pub. of Cited Doc. (mm-dd-yyyy)	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
	AA	4,692,781		Rountree et al.	09/08/1987	
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	AG					
	AH					
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Exam. Initials*	Cite No.[1]	Foreign Patent Document Office[3]	Foreign Patent Document Number[4]	Foreign Patent Document Kind Code[2] (if known)	Name of Patentee or Applicant of Cited Doc.	Date of Pub. of Cited Doc. (mm-dd-yyyy)	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	T[6]
	BA							
	BB							
	BC							
	BD							
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	BF							
	BG							
	BH							
	BI							
	BJ							

OTHER PRIOR ART - NON PATENT LITERATURE DOCUMENTS

Exam. Initials*	Cite No.[1]	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T[2]
	CA	Rountree et al., "A Process-Tolerant Input Protection Circuit for Advanced CMOS Processes," 1988 EOS/ESD Symposium, pp. 201-05	
	CB	Duvvury et al., "Substrate Pump NMOS for ESD Protection Applications," 2000 EOS/ESD Symposium, Paper 1A.2.1, pp. 7-17	
	CC	Kunz et al., "5-V Tolerant Fail-safe ESD Solutions for 0.18 um Logic CMOS Process," 2001 ESD/EOS Symposium, September 11, 2001	
	CD		
	CE		
	CF		
	CG		
	CH		
	CI		
	CJ		

Examiner Signature	A. Jackson	Date Considered	6-10-04

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[1]Unique citation designation number. [2]Applicant is to place a check mark here if English Translation is attached.